

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method of improving a physical design of a current integrated circuit, comprising the steps of:

- a) receiving a netlist of said current integrated circuit;
- b) receiving physical design information from a prior integrated circuit; and
- c) generating said physical design based on said netlist and said physical design information.

2. (Original) A method as recited in Claim 1 wherein said physical design information includes pin assignments of blocks of said prior integrated circuit.

3. (Original) A method as recited in Claim 1 wherein said physical design information includes optimal clock distribution tree of said prior integrated circuit.

4. (Original) A method as recited in Claim 1 wherein said physical design information includes parasitic extraction data of said prior integrated circuit.

5. (Original) A method as recited in Claim 1 wherein said physical design information includes locations of obstructions of said prior integrated circuit.

6. (Currently amended) A method as recited in Claim 5 wherein said obstructions ~~includes~~ include a random access memory (RAM).

7. (Original) A method as recited in Claim 1 wherein said physical design information includes identification of congested blocks of said prior integrated circuit.

8. (Original) A method as recited in Claim 1 wherein said physical design information includes metal resources of said prior integrated circuit.

9. (Original) A method as recited in Claim 1 wherein said physical design information includes information which facilitates optimizing said current integrated circuit.

10. (Original) A method as recited in Claim 1 wherein said step c) includes:

generating a top-level physical design of said current integrated circuit using said netlist and said physical design information including block-level physical design information of said prior integrated circuit.

11. (Original) A method as recited in Claim 1 wherein said step c) includes:

generating a block-level physical design of said current integrated circuit using said netlist and said physical design information including block-level physical design information of said prior integrated circuit.

12. (Original) A method as recited in Claim 1 wherein said physical design is an abutted-pin hierarchical physical design including a top-level physical design and a block-level physical design.

13. (Original) A method as recited in Claim 1 wherein said step c) includes:

partitioning said netlist into a plurality of blocks, each block including a block-level netlist;

performing a top-level floor planning;

performing a top-level placement and route for a plurality of top-level objects;

performing a top-level placement and route for a plurality of ports from said blocks to determine pin assignments for each block; and

generating and optimizing a block-level physical design for each block in parallel.

14. (Original) A method as recited in Claim 13 wherein said generating and optimizing includes:

pressing each portion of each top-level object, which is located within a boundary of a particular block, into said particular block;

generating each pin for each block based on said top-level placement and route to determine pin assignments;

performing a block-level floor planning for each block;

performing a block-level placement for each block;

performing a plurality of block-level operations to optimize each block;

and

performing a block-level route for each block.

15. (Original) A computer-readable medium comprising computer-executable instructions stored therein for performing a method of improving a physical design of a current integrated circuit, said method comprising:

- a) receiving a netlist of said current integrated circuit;
- b) receiving physical design information from a prior integrated circuit; and;
- c) generating said physical design based on said netlist and said physical design information.

16. (Original) A computer-readable medium as recited in Claim 15 wherein said physical design information includes pin assignments of blocks of said prior integrated circuit.

17. (Original) A computer-readable medium as recited in Claim 15 wherein said physical design information includes optimal clock distribution tree of said prior integrated circuit.

18. (Original) A computer-readable medium as recited in Claim 15 wherein said physical design information includes parasitic extraction data of said prior integrated circuit.

19. (Original) A computer-readable medium as recited in Claim 15 wherein said physical design information includes locations of obstructions of said prior integrated circuit.

20. (Currently amended) A computer-readable medium as recited in Claim 19 wherein said obstructions ~~includes~~ include a random access memory (RAM).

21. (Original) A computer-readable medium as recited in Claim 15 wherein said physical design information includes identification of congested blocks of said prior integrated circuit.

22. (Original) A computer-readable medium as recited in Claim 15 wherein said physical design information includes metal resources of said prior integrated circuit.

23. (Original) A computer-readable medium as recited in Claim 15 wherein said physical design information includes information which facilitates optimizing said current integrated circuit.

24. (Original) A computer-readable medium as recited in Claim 15 wherein said step c) includes:

generating a top-level physical design of said current integrated circuit using said netlist and said physical design information including block-level physical design information of said prior integrated circuit.

25. (Original) A computer-readable medium as recited in Claim 15 wherein said step c) includes:

generating a block-level physical design of said current integrated circuit using said netlist and said physical design information including block-level physical design information of said prior integrated circuit.

26. (Original) A computer-readable medium as recited in Claim 15 wherein said physical design is an abutted-pin hierarchical physical design including a top-level physical design and a block-level physical design.

27. (Original) A computer-readable medium as recited in Claim 15 wherein said step c) includes:

partitioning said netlist into a plurality of blocks, each block including a block-level netlist;

performing a top-level floor planning;

performing a top-level placement and route for a plurality of top-level objects;

performing a top-level placement and route for a plurality of ports from said blocks to determine pin assignments for each block; and

generating and optimizing a block-level physical design for each block in parallel.

28. (Original) A computer-readable medium as recited in Claim 27 wherein said generating and optimizing includes:

pressing each portion of each top-level object, which is located within a boundary of a particular block, into said particular block;

generating each pin for each block based on said top-level placement and route to determine pin assignments;

performing a block-level floor planning for each block;

performing a block-level placement for each block;

performing a plurality of block-level operations to optimize each block;

and

performing a block-level route for each block.

29. (Original) A method of determining a plurality of pins for each block of a physical design of a current integrated circuit, comprising:

a) receiving a netlist of said current integrated circuit;

b) receiving physical design information from a prior integrated circuit, wherein said physical design information includes pin assignments of blocks of said prior integrated circuit;

c) using said netlist and said physical design information to perform a top-level placement for a plurality of ports corresponding to each block of said current integrated circuit;

d) using said netlist and said physical design information to perform a top-level route for said ports to determine pin assignments for each block of said current integrated circuit; and

e) generating each pin for each block based on said top-level route to determine pin assignments.

30. (Original) A method as recited in Claim 29 wherein said physical design is an abutted-pin hierarchical physical design.

31. ((Original) A method as recited in Claim 30 wherein said physical design includes a top-level physical design.

32. (Original) A method as recited in Claim 30 wherein said physical design includes a block-level physical design.

33. (Original) A method as recited in Claim 29 further comprising:
partitioning said netlist into a plurality of blocks of said current integrated circuit, each block including a block-level netlist.

34. (Original) A method as recited in Claim 29 wherein said physical design information includes optimal clock distribution tree of said prior integrated circuit.

35. (Original) A method as recited in Claim 29 wherein said physical design information includes parasitic extraction data of said prior integrated circuit.

36. (Original) A method as recited in Claim 29 wherein said physical design information includes locations of obstructions of said prior integrated circuit.

37. (Currently amended) A method as recited in Claim 36 wherein said obstructions ~~includes~~ include a random access memory (RAM).

38. (Original) A method as recited in Claim 29 wherein said physical design information includes identification of congested blocks of said prior integrated circuit.

39. (Original) A method as recited in Claim 29 wherein said physical design information includes metal resources of said prior integrated circuit.

40. (Original) A method as recited in Claim 29 wherein said physical design information includes information which facilitates optimizing said current integrated circuit.

41. (Original) A computer-readable medium comprising computer-executable instructions stored therein for performing a method of determining a plurality of pins for each block of a physical design of a current integrated circuit, comprising:

- a) receiving a netlist of said current integrated circuit;
- b) receiving physical design information from a prior integrated circuit, wherein said physical design information includes pin assignments of blocks of said prior integrated circuit;
- c) using said netlist and said physical design information to perform a top-level placement for a plurality of ports corresponding to each block of said current integrated circuit;
- d) using said netlist and said physical design information to perform a top-level route for said ports to determine pin assignments for each block of said current integrated circuit; and
- e) generating each pin for each block based on said top-level route to determine pin assignments.

42. (Original) A computer-readable medium as recited in Claim 41 wherein said physical design is an abutted-pin hierarchical physical design.

43. (Original) A computer-readable medium as recited in Claim 42 wherein said physical design includes a top-level physical design.

44. (Original) A computer-readable medium as recited in Claim 42 wherein said physical design includes a block-level physical design.

45. (Original) A computer-readable medium as recited in Claim 41 wherein said method further comprises:

partitioning said netlist into a plurality of blocks of said current integrated circuit, each block including a block-level netlist.

46. (Original) A computer-readable medium as recited in Claim 41 wherein said physical design information includes optimal clock distribution tree of said prior integrated circuit.

47. (Original) A computer-readable medium as recited in Claim 41 wherein said physical design information includes parasitic extraction data of said prior integrated circuit.

48. (Original) A computer-readable medium as recited in Claim 41 wherein said physical design information includes locations of obstructions of said prior integrated circuit.

49. (Currently amended) A computer-readable medium as recited in Claim 41-~~48~~ wherein said obstructions ~~includes~~ include a random access memory (RAM).

50. (Original) A computer-readable medium as recited in Claim 41 wherein said physical design information includes identification of congested blocks of said prior integrated circuit.

51. (Original) A computer-readable medium as recited in Claim 41 wherein said physical design information includes metal resources of said prior integrated circuit.

52. (Original) A computer-readable medium as recited in Claim 41 wherein said physical design information includes information which facilitates optimizing said current integrated circuit.